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09/702,202	10/30/2000	Peter Korger	5201-23000	9450

			EXAMINER
24319	7590	07/28/2004	THOMAS, SHANE M

LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106 LEGAL
MILPITAS, CA 95035

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Please find below and/or attached an Office communication concerning this application or proceeding.

| | Application No. 09/702,202 | Applicant(s) KORGER, PETER |
| **Office Action Summary** | Examiner Shane M Thomas | Art Unit 2186 |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

　　4a) Of the above claim(s) *3,4,11 and 17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-10,12-16 and 18-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

　　Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

　　Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

　　a)☐ All　b)☐ Some * c)☐ None of:

　　　1.☐ Certified copies of the priority documents have been received.

　　　2.☐ Certified copies of the priority documents have been received in Application No. _____ .

　　　3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

　　* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ .

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____ .

DETAILED ACTION

Drawings

The Examiner's previous objections to the drawings (figure 1a) have been respectfully withdrawn hereto.

Specification

The disclosure is objected to because of the following informality:

The Examiner objects to the indication that identifies Applicant's figure 1a and 1b as --typical-- storage device (page 5, lines 7-8, of the disclosure). Such a term could be interpreted as leading one to believe the figures are commonly found and known in the art. Because the Applicant does not wish to label the respective figures as --prior art--, the Examiner recommends amending page 5, lines 7-8, to reflect this notion. Specifically, the Examiner would entertain an amendment to the lines as follows:

"Figs. 1a and 1b illustrate the organization of a ~~typical~~ storage device, such as a first-in first-out (FIFO) buffer <u>as pertaining to the present invention,</u>" or the like.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The Examiner previous rejections of claims 5-9 under §112, second paragraph, have been respectfully withdrawn hereto.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth
> in section 102 of this title, if the differences between the subject matter sought to be patented and the prior
> art are such that the subject matter as a whole would have been obvious at the time the invention was made
> to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be
> negatived by the manner in which the invention was made.

Upon further consideration, the Examiner has respectfully withdrawn the previous

rejections of claims 1,2,5,6,10,12,13, and 14 under §103(a) as being unpatentable over Williams

et al. (U.S. Patent No. 6,408,409) in view of the Applicant's admitted prior art.

Claims **1, 2, and 5** are rejected under 35 U.S.C. 103(a) as being unpatentable over

Murphy (U.S. Patent No. 6,433,787) in view of the Applicant's admitted prior art (herein APA).

As per claim **1**, Murphy shows a memory system in figure 3 comprising a FIFO buffer

320 and a storage device 350, consisting of N storage locations, each storage location having a

corresponding read/write flag bit 352. Since each entry contains a flag field, it can be seen that

there are a total of N flag fields. When a corresponding read/write flag is valid (True) for the

entry of the storage device 350 to be written to, the write logic 330 stalls until the flag is cleared

by the read logic 360. When the write completes, the flag is set to True (see column 4, lines 16-

19). Likewise, when an entry in the storage device is False, the read process stalls and waits for

data to be written. After the location is marked valid by the write process, the data is then read

out by the read logic and the flag bit is set to False (column 4, lines 24-26).

As per lines 5-8, Murphy does not specifically show an N-bit read register and an N-bit

write register associated with each entry of the storage device 350. Instead, Murphy teaches

using a single validity flag for each entry as taught in column 8, lines 3-36. While Murphy does

not teach the structure as claimed by the Applicant, it can be seen by one having ordinary skill in

the art that the function of the read bit, write bit, and respective logic gate associated with the

read bit and write bit pair exuded equal performance. The Applicant states in the Summary of

the invention (page 2, lines 1-2) that the output of each XOR gate (logic gate) is simply used to

determine if the corresponding entry of a storage system is valid. Similarly, the validity flag 352

of Murphy can be seen as performing in an identical fashion as the output of the XOR gate of the

Applicant. It would have been obvious to one having ordinary skill in the art at the time the

invention was made to have utilized the teaching of the validity flag bit over the read bit, write

bit, and XOR gate combination as claimed by the Applicant when determining the validity of an

entry in a storage device. Using the single validity flag of Murphy instead of the teaching of the

Applicant would have resulted in less memory [space] being utilized (1 bit of Murphy compared

to 2 bits - one read and one write - for the Applicant) thus saving valuable chip space and further,

would have resulted in an overall faster performance of the storage system when trying to

determine the validity of an entry of a storage device. The Applicant's claimed invention would

have needed extra time to propagate the result of the XOR of the read and write bits for an entry

to deem an entry valid, while the prior art teaching of Murphy would not need a logic gate.

Murphy does not explicitly state that the data being read into the memory system 300

from bus 305 contains tag bits. Applicant's admitted prior art states on page 2, line 5, that *it is*

often advantageous to include tag bits along with the data when being written into a FIFO

structure. One function of the prior art tags bits as admitted by the applicant is to assist in data

transfers, since *less processing is required at the receiving end to ascertain the nature of the*

transfer (page 2, line 9). Therefore, it would have been obvious to one of ordinary skill in the art

at the time the invention was made to modify the storage device 350 of Murphy to incorporate

tag bit storage locations. Doing so would have helped to alleviate some of the --overhead-- bytes

that contain addressing information usually sent with every pixel-byte over a graphic system bus

(see column 1, line 62, thru column 2, line 5). This process would have further supported the

"burst-transaction" mentioned by Murphy in column 2, lines 8-9; the tag bits could have been

used for further aiding in specifying a chain of several related pixel-bytes to a destination, or

used for verification purposes to have made sure the chain of pixel-bytes were sent to the correct

area of the system that requested the pixels, after being read out of the memory device 300 of

Murphy.

As per claim **2**, the modified memory system 300 of Murphy does not explicitly state that

data is written to and read out of the system using different clock cycles. However as is known

in the art, and admitted by the applicant on page 1, line 25, FIFO systems often employ different

clocks for reading and writing data. The dual-clock system is especially useful for "burst mode"

data transfers (line 26). One embodiment of the memory system of Murphy is for use in a

graphics system with pixel data being transferred through the system. Murphy's modified

memory system would have been useful in the video camera example presented by the applicant

in line 27. It would have been obvious to one in the art at the time the invention was made to

utilize the memory system of Murphy in the video camera system in order for pixel data to be

written into the memory system by the camera, and then read out by a slower clock of another

system, such as a computer as admitted by the applicant on page 2, line 1.

As per claim **5**, the Examiner will refer to storage locations of storage device 350 that have been written to but not read (read/write bit 352 is True) as --valid-- storage locations.

Claims **6-8, 10, 12-16, 18 and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy (U.S. Patent No. 6,433,787) in view of APA in further view of Zaidi et al. (U.S. Patent No. 5,574,689).

As per claims **6,7,14 and 15**, the modified memory system 300 of Murphy lacks a way to compare valid tag bits across every storage location of storage device 350. As was stated by the applicant, the tag bits of a system could be used to denote the particular I/O device a packet of data originated from. Further the applicant states that this tag system is beneficial in that it would be possible to determine whether the FIFO contained data from a specific I/O device without have to read each entry in the queue (page 7, lines 14-19). Using the case of a particular I/O device (e.g. videocamera of the above mentioned example) sending data packets to the graphic system (figure 6) of Murphy, the graphics system may want or require information regarding which pixels, corresponding to different I/O devices, are in the memory system 300. One reason for this need could be to store the expectant data into a buffer dedicated to a particular I/O device (see applicant's admitted prior art page 7, lines 17-19). Thus it would have been useful to determine the tag information of the --valid-- storage locations. Only tag bits corresponding to the "valid" locations would be useful since the data associated with the --invalid-- locations would have either been previously read out or not yet written into the storage device 350 by the write logic.

Zaidi shows in figure 2 that an AND gate 212 can be used to transfer tag information

from a queue 200. The --tag-- bit in figure 2 is being used as a valid bit and is ANDed with a

logic mask 214. As is known in the art, the mask is used to determine if in fact the tag bit is

valid by ANDing it with a logic 1. Therefore, it would have been obvious to one of ordinary

skill in the art at the time the invention was made to further modify the memory system of

Murphy to have included the AND gates used by Zaidi to determine the validity of tag bits in

each storage location. Instead of a valid entry mask 214 being used by Murphy (as the other

input into the tag bit AND gate) to determine a valid tag bit of a storage location, the read/write

flag bit 352 of the corresponding storage location would have been used since the read/write flag

would have been a logic 1 if and only if the storage location was --valid-- (data in the storage

location had not yet been read out). Since N storage locations comprise storage device 350, N

AND gates would have been used for *each* tag bit because it would have been necessary to

analyze the tag bits of each storage location when determining which tag bits are --valid-- tag

bits (i.e. corresponding to --valid-- storage locations).

As per claims **8** and **19**, now that every tag bit of every storage location has been

determined to be --valid-- or not, Murphy does not have logic to further determine which tag bits

are --valid-- *across* the storage device. The applicant's admitted prior art, figure 1b, and page 7,

lines 11-14, state that a series of OR gates can be used to simultaneously determine if the logic

level of any of the tag bits are --valid--. Therefore, it would have been obvious to one having

ordinary skill in the art at the time the invention was made to further modify the memory system

of Murphy to have utilized OR gates connected to the output of the tag bits' AND gates in order

to determine which, if any, of the tag bits are active or --valid-- in the memory system. Referring

to the previous example stated above of the graphic system of Murphy utilizing tag bits to

identify the I/O device a data packet corresponding to a particular location of the storage device

had originated from, it would have been seen that the output of the OR gates would have

effectively determined which device (based on the tag bits) from which data residing in the valid

locations of the storage device had originated from.

As per claim **10**, the Examiner is referring to the storage device 350 (which includes flag

bits 352) as a --first-in-first-out-- (FIFO) system. This is validated since for a system writing

data to memory system 300 with consecutive offset addresses, no reordering would be needed.

Therefore the first data segment read into the memory system 300 will be the first segment

written to the --FIFO-- storage system 350 (from buffer 320) and thus the first segment *read* out

of the --FIFO-- storage system will be that same data segment.

Regarding claim 10, the same rejections as claims 1, 2, and 8 are applied. The rejection

of claim 1, lines 1-4 is applied to lines 1-3 and lines 6-8. The rejection of claim 2 is applied to

lines 4-5. The rejection of claim 8 is applied to lines 7-8. The rejection of claim 8 shows how

every tag bit of the storage device 350 of Murphy would have been ANDed with the

corresponding read/write flag bit 352 to determine which tag bits correspond to a valid storage

location (location that has been written to but no read from). The Examiner is regarding the

validity or invalidity of the tag bits as the --status-- of the tag bits.

As per claim **12**, the rejection follows the rejection for claim 1, lines 5-8, in that Murphy

does not need combinatorial logic to determine which FIFO locations have been written to and

not read. Similarly, a True indication in the validity flag field 352 corresponding to a respective

entry that has been written but no read (column 8, lines 3-36).

As per claim **13**, the rejection follows the rejection of claim 5.

As per claim **16**, the rejection for claim 1, line 2, is applied to line 3. The rejection for

lines 8-16 follows the rejection of claim 1, lines 5-8. The rejection for claim 2 is applied to lines

4-6. Murphy teaches lines 8-16 by using a single validity bit, as discussed in the rejection of

claim 1, and the toggling of the validity for reading and writing in column 8, lines 3-36. The

rejection for line 17 follows the rejection for claims 6 and 7 with the Examiner defining

--detecting active tag bits-- as using combinatorial logic to only compare tags bits of --valid--

storage locations. The rejection of claim 8 is applied to lines 18-19 since a logic signal is

generated from the output of the OR gates corresponding to each tag bit in the --FIFO--.

As per claim **18**, the rejection of lines 3-4 follows the rejection for claim 1, lines 5-8. In

the discussion for the rejection of claim 1, line 5-8, the Examiner noted that Murphy does not

need to compare the --first and second register flags-- in order to determine if the data in the

respective entry is valid. Murphy uses the single validity flag bit 352 to perform this --equal

performance-- measure in order to determine validity. The rejection of lines 5-6 follows the

rejection of claim 7.

Claims **9 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy

Murphy (U.S. Patent No. 6,433,787) in view of APA in further view of Zaidi (U.S. Patent No.

5,574,689) in further view of Klingelhofer (U.S. Patent 5,884,099). Since reading and writing

can occur at synchronous intervals, but not necessarily synchronous with each other, it would

have been beneficial to synchronize the output of the ORed valid tag signals so that the read

logic of Murphy (360 figure 3) could have gathered the --status-- of the tag bits corresponding to

data that had been written but not read out and had this information available for the read logic at the same time the read logic had determined what location to read out. Non-synchronous behavior between the valid tag signals and the read logic could have resulted in the read logic losing "valid" tag information since the result of the combinatorial logic may have come after the read logic begin accessing a storage location was read out. As stated above, this tag information could have been used to send specific data to a buffer dedicated to a specific I/O device (applicant's admitted prior art, page 7, line 18). Figure 1 of Klingelhofer shows synchronization circuitry 136 and teaches that this circuitry adjusts the output of the FIFO flag circuitry to be synchronous with the output clock 116 to enable output from the FIFO (column 3, lines 61-63). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Murphy to include the output synchronization of Klingelhofer so that the read circuitry would have been synchronous with the output of the valid tag OR gates. This crucial modification would have been able to overcome the aforementioned problem of losing valid tag data. With Klingelhofer's teaching, the read logic would clock in the tag bit information when the combinatorial logic had produced a valid calculation for the tag bits of the storage system.

Response to Arguments

The rejection of claims 1,2,5,6,10,12,13, and 14 under §103(a) as being unpatentable over Williams et al. (U.S. Patent No. 6,408,409) in view of the Applicant's admitted prior art has been respectfully withdrawn.

Applicant's arguments with respect to claims 1,2,5-10, 12-16 and 18-20 have been considered but are moot in view of the new grounds of rejection.

The indicated allowable subject matter of claims 7-9,15,16,and 18-20 have been withdrawn in view of the different interpretation of the prior art of record.

To clarify the record regarding the indication of the miscommunication of allowable subject matter regarding the Applicant's arguments on page 6-7 of the amendment filed 2 April 2004, the Examiner restates the point made in the Advisory Action, mailed 13 April 2004 regarding amended claim 1. Further, the amendment filed 18 November 2003, changed the scope of claim 10 to incorporate --N-bit read and N-bit write registers--. However, these arguments are moot in view of the new grounds of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M Thomas whose telephone number is (703) 605-0725. The examiner can normally be reached on M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane M. Thomas

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100